Amendments to the Claims

1. (Currently Amended) Continuous-time filter system ~~with self-calibration means, the system~~ comprising a master control unit (36) and a slave unit with at least one slave filter (27.1 – 27.n),

- the master control unit (36) comprising
- an integrator (30) having ~~circuit elements (33, C)~~ a transconductor and a capacitor which match those elements of the slave filter (27.1 – 27.n) that define the slave filter's time constant (τ),
- a voltage comparator (35) connected to an output (34) of the integrator (30), the voltage comparator (35) providing an output frequency signal (f_{com}), and
- a phase frequency comparator (PFC; 28) providing a control signal (υ) as output signal, the phase frequency comparator (PFC; 28) receiving said output frequency signal (f_{com}) and a reference frequency signal (f_{ref}) as input signals,
- the slave unit comprising said at least one slave filter (27.1 – 27.n), the slave filter (27.1 – 27.n) having a control signal input (41) for receiving said control signal (υ) thus allowing to calibrate the slave filter's transfer function by influencing the slave filter's time constant (τ).

2. (Original) The system of claim 1, wherein the slave filter is an RC-filter and the control signal (υ) is a discrete signal leading to a calibration of the slave filter's transfer function in steps.

3. (Original) The system of claim 1, wherein the slave filter is a continuous-time Gm-C-filter and the control signal (υ) is a continuous signal.

4. (Currently Amended) The system of claim 1, ~~2 or 3,~~ wherein the slave filter is an integrated filter.

5. (Currently Amended) The system of claim 1 ~~one of the preceding claims~~, wherein the master control ~~block~~ unit (36) comprises one transconductor (33) and one capacitor (C) only.

6. (Currently Amended) The system of claim 1 ~~one of the preceding claims~~, wherein the phase frequency comparator (PFC; 28) comprises:

- a loop filter (52) providing the control signal (υ) as output signal,
- a phase frequency detector (PFD; 53) situated in front of the loop filter (52), the phase frequency detector (PFD; 53) receiving said output frequency signal (f_{com}) and a reference frequency signal (f_{ref}) as input signals,
- an error signal (x) representing the phase difference between the output frequency signal (f_{com}) and the reference frequency signal (f_{ref}) being fed by the phase frequency detector (PFD; 53) to the loop filter (52).

7. (Currently Amended) The system of claim 1 ~~one of the preceding claims~~, wherein the master control unit (36) comprises a switch (39) being controllable by a signal (V_S).

8. (Canceled)

9. (Currently Amended) The system of claim 1 ~~one of the preceding claims~~, wherein a DC voltage (V_B) is applied to an input (32) of the integrator (30).

10. (Currently Amended) The system of claim 1 ~~one of the preceding claims~~, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying

- a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35), and/or
- a DC voltage (V_B) being applied to an input (32) of the integrator (30), and/or
- the frequency (f_{CK}) of a clock signal (CK).

11. (Canceled)

12. (Currently Amended) The system of claim 1 ~~one of the claims 1 through 9~~, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying a DC voltage (V_B) being applied to an input (32) of the integrator (30) while keeping a threshold voltage (V_{th}) being applied to an input of the voltage comparator (35) and the reference frequency signal (f_{ref}) unchanged.

13. (Currently Amended) The system of claim 1 ~~one of the claims 1 through 9~~, wherein the integrator (30) has a transconductance (Gm) that can be tuned by varying a threshold

voltage (V_{th}) being applied to an input of the voltage comparator (35) while keeping a DC voltage (V_B) being applied to an input (32) of the integrator (30) and the reference frequency signal (f_{ref}) unchanged.

14. (Currently Amended) The system of claim 1, wherein the ~~master control block (36)~~ transconductor comprises a voltage-to-current converter (VCC; 60) ~~and/or~~ that includes one of a programmable resistor array (PRA) ~~and/or~~ or a programmable capacitor array.

15. (Currently Amended) The system of claim 1, further embodied in a telecommunication ~~Telecommunication~~ system, video-signal processing system, or disk driver system ~~comprising a system in accordance with at least one of the claims 1 through 14~~.

16. (New) Continuous-time filter system comprising a master control unit and a slave unit with at least one slave filter,

the master control unit comprising:

an integrator having a transconductor and a capacitor that match those elements of the slave filter that define the slave filter's time constant (τ),

a voltage comparator connected to an output of the integrator, the voltage comparator providing an output frequency signal, and

a phase frequency comparator providing a control signal (υ) as output signal, the phase frequency comparator receiving said output frequency signal and a reference frequency signal as input signals; and

the slave unit comprising said at least one slave filter, the slave filter having a control signal input for receiving said control signal (υ) thus allowing to calibrate the slave filter's transfer function by influencing the slave filter's time constant (τ),

wherein the master control unit comprises a switch being controllable by a signal (V_S), and wherein a logic circuit is employed in order to provide the signal (V_S) and the reference frequency signal from a clock signal.

17. (New) Continuous-time filter system comprising a master control unit and a slave unit with at least one slave filter,

the master control unit comprising:

an integrator having a transconductor and a capacitor that match those elements of the slave filter that define the slave filter's time constant (τ),

a voltage comparator connected to an output of the integrator, the voltage comparator providing an output frequency signal, and

a phase frequency comparator providing a control signal (υ) as output signal, the phase frequency comparator receiving said output frequency signal and a reference frequency signal as input signals; and

the slave unit comprising said at least one slave filter, the slave filter having a control signal input for receiving said control signal (υ) thus allowing to calibrate the slave filter's transfer function by influencing the slave filter's time constant (τ),

wherein the integrator has a transconductance that can be tuned by varying an input clock frequency of a clock signal while keeping a threshold voltage being applied to an input of the voltage comparator and a DC voltage being applied to an input of the integrator unchanged.